Designing with the Si9174, Si9175 and Si9176 Family of High-Performance Synchronous Step-Down Converters

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INTRODUCTION

The Si9174, Si9175 and Si9176 are high-efficiency, internally compensated 600-mA synchronous step-down (buck) converters designed to convert a 2.6-V to 6.0-V input voltage to a regulated dc output voltage. Internal compensation and a *2-MHz switching* frequency reduce the number and size of external components, conserving board space. Synchronous rectification allows for higher efficiency as compared to designs that rely on a Schottky diode. All of this simplifies design and construction of a low-cost, small, fast-response, high-frequency dc-to-dc power supply ideally suited to battery and portable applications.

THE Si9174, Si9175, Si9176 FAMILY DESCRIPTION

The family is based on a core architecture that includes a 2-MHz synchronous PWM mode of operation, a PSM mode of operation, an “Auto” mode of operation, internal loop compensation, converter shutdown, overcurrent protection, and thermal shutdown.

The following individual feature sets differentiate the members of the family. The Si9174 has a dynamically adjustable output voltage controlled by the voltage on the DAC pin and allows synchronization of the internal oscillator with a 13-MHz external signal. The Si9175 is a fixed-output voltage converter with synchronization capability, while the Si9176 provides a fixed-voltage output without synchronization capability. Figure1 shows the typical application schematics.

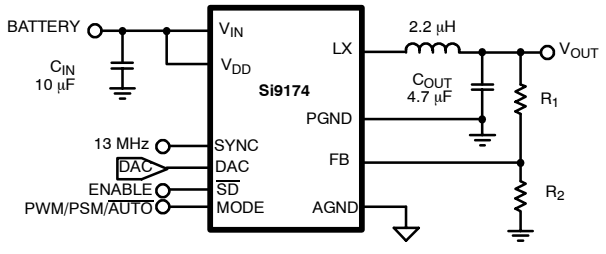


Figure 1. Si9174 Typical Schematic

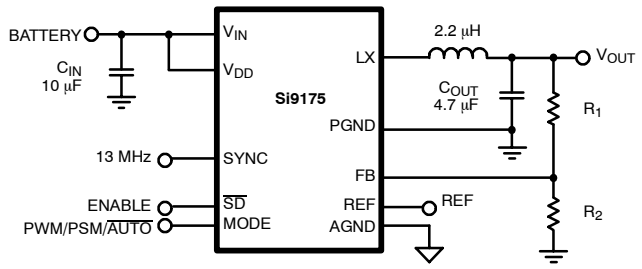


Figure 2. Si9175 Typical Schematic

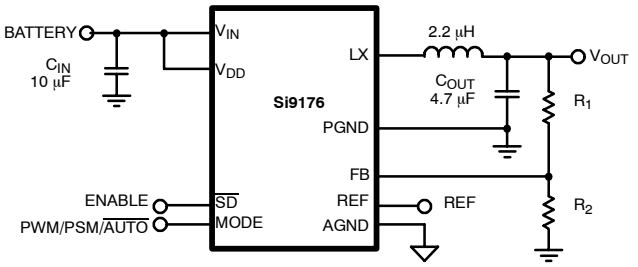


Figure 3. Si9176 Typical Schematic

OPERATIONAL DESCRIPTION

Start-Up

When voltage is applied to the V_{IN} pin, the undervoltage lockout (UVLO) circuit prevents the controller’s output switches and oscillator circuit from turning on until the voltage on the V_{IN} pin exceeds 2.4 V. Provided the V_{IN} pin is above this threshold, startup occurs when $\overline{SD}$ pin is raised to the HIGH level. The converter operates continuously unless the voltage on V_{IN} drops below 2.3 V or $\overline{SD}$ is set to a LOW level. UVLO hysteresis prevents the converter from dropping in-and-out of start-up, unintentionally locking up the system. The $\overline{SD}$ pin can be connected to the V_{IN} pin if shutdown mode is not required. The output response can be seen in Figure 4. Startup from a shutdown condition with V_{IN} applied is seen in Figure 5. In both methods, the output is established in about 50 µs with a resistive load of 4 Ω.

Startup is always performed in PWM mode but the operating mode will change to other modes depending upon the MODE pin and the peak inductor current.

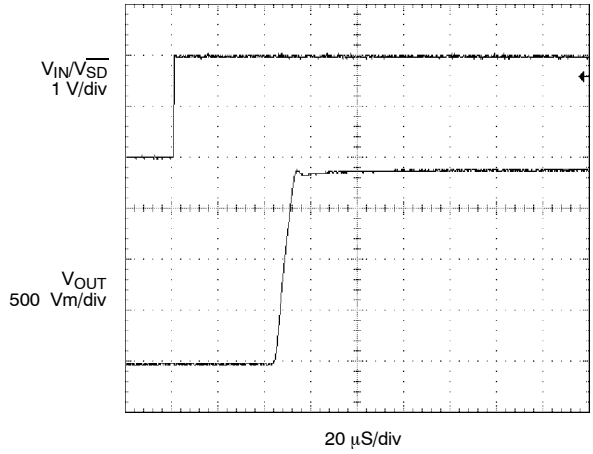


Figure 4. Start-Up: MODE = High, $V_{IN} = \overline{V_{SD}}$, $R_{LOAD} = 4\ \Omega$

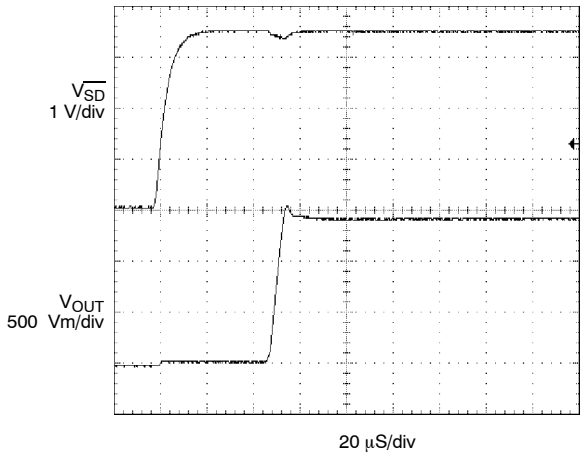


Figure 5. Start-Up: $V_{IN} = 3.6$ V, $R_{LOAD} = 4\ \Omega$

Mode Control

The Si9174/75/76 have three distinct modes of regulator operation controlled by the MODE pin. These are forced pulsewidth modulation (PWM) for high-current loads, forced pulse skipping modulation (PSM) for low-current loads, and AUTO mode to allow automatic transition between PWM and PSM for high- and low-current loads.

Forced PWM Mode (Pin 6 MODE = HIGH)

When the Mode pin is in the logic HIGH condition, the Si9174/75/76 family devices operate as voltage-mode, 2-MHz PWM step-down regulators with synchronous rectification. PWM mode provides the best efficiency when load currents are in excess of 150 mA.

At the beginning of each clock cycle, the high-side p-channel MOSFET (PMOS) is switched on. This establishes current flow through the inductor to the load. When the internal oscillator ramp exceeds the output of the error amplifier, the high-side MOSFET is turned off, and, after a break-before-make timeout, the n-channel synchronous MOSFET (NMOS) is turned on. Since the inductor will maintain current flow, current now flows through the synchronous MOSFET, thereby continuing to provide current to the load. When the clock cycle is completed, the synchronous MOSFET will turn off and the next clock cycle begins. The use of a synchronous MOSFET increases efficiency. The increase in efficiency is due to a reduced voltage drop across the MOSFET as compared to the voltage droop across the conventional freewheeling Schottky diode.

The maximum duty cycle of the Si9174/75/76 family is 100% in PWM mode. This allows designers to extract the maximum stored energy in the battery. When V_{IN} drops to V_{OUT} + 150 mV for a 600-mA load, the duty cycle will shift from about 98% to 100% duty cycle, making the IC behave like a 0.3-Ω load switch. If V_{IN} then exceeds V_{OUT} by about 190 mV, the IC will restart into PWM mode at about 97% duty cycle.

During each cycle, the p-channel MOSFET switch is current-limited to 1.5 A (typical) to protect the IC while continuing to supply up to 600 mA to the load. In the Si9174, the n-channel synchronous MOSFET switch is internally current limited to 1.5 A (typical) during the negative output voltage transients as slewed by the DAC pin.

The Si9174/5/6 ICs are voltage-mode converters. In voltage mode, the output voltage is regulated by modulation of the duty cycle in PWM mode. This single control loop is internally compensated to provide excellent input voltage and load current transient response (<50 μs), a fixed noise spectrum, and zero-to full-load current capability with low output ripple (5 mV).

Forced PSM Mode (Pin 6 MODE = OPEN)

By leaving the MODE pin open-circuit, the converter runs in pulse skipping modulation (PSM) mode. PSM mode is used to increase efficiency under light load conditions and does not offer any efficiency advantage over PWM mode when the load exceeds 150 mA. The PSM mode switching frequency will vary with input voltage and load conditions. The minimum PSM frequency for a 30-mA load is 20 kHz to prevent the switching noise in the audible frequency range.

The efficiency advantage of PSM mode at light load conditions is gained from providing energy transfer cycles only as needed. A lower switching frequency reduces the gate charge loss produced by the input capacitance of the internal MOSFET switches, the switch resistive losses, and the inductor resistive loss. In PSM mode, the oscillator continues to operate, but an energy transfer cycle occurs only if the FB pin voltage is below the DAC (Si9174) or REF voltage (Si9175/6) at the start of each clock cycle. When the p-channel MOSFET is turned on, the inductor current is allowed to reach the peak current threshold of 300 mA. The p-channel MOSFET

is then turned off and the n-channel MOSFET is turned on. Unlike PWM mode, the n-channel MOSFET switch turns off as the inductor current approaches zero-current.

As in PWM mode, the maximum duty cycle in PSM mode of the Si9174/75/76 is 100% and permits maximum utilization of stored energy in the battery. The duty cycle will transition smoothly from 99% to 100% when V_{IN} drops to V_{OUT} + 50 mV at a 150-mA load. When V_{IN} exceeds V_{OUT} by about 100 mV, the IC transitions into PSM mode at about 98% duty cycle.

Auto Mode (Pin 6 MODE = Low)

When the MODE pin is grounded, the Si9174/75/76 automatically switches between PWM mode and PSM mode. For heavy loads, the converter operates in PWM mode to achieve maximum efficiency. With light loads, the converter operates in PSM mode to conserve power. The switchover threshold between the two modes is determined by the peak inductor current, which is 300 mA nominal. The peak inductor current is *not* the load current but is related to load current, input/output voltage, and inductance. PWM mode operation continues as long as inductor current exceeds the threshold. If the peak inductor current does not reach the threshold, the regulation mode switches to PSM mode. The PSM-to-PWM mode switchover threshold current for increasing load currents is higher than that of the PWM-to-PSM mode switchover threshold for decreasing load currents. There is hysteresis in the switchover threshold to provide smooth mode transitions.

In Auto Mode the maximum duty cycle is 100% and operation is the same as the forced PWM and forced PSM modes described above.

Oscillator Synchronization (Pin 8 Si9174 and Si9175)

The Si9174 and Si9175 have the capability of synchronizing the internal oscillator to an external clock to control system noise spectrum. Typically, this is an ac-coupled 13-MHz, 0.5-V_{P-P} sine wave, although the IC will synchronize to a 10- to 15-MHz sine or square wave. An on-chip divide-by-six circuit sets the converter switching frequency to one sixth of the applied signal. The functional block diagram in Figure 4 shows this feature. This pin must not be allowed to float since there are no internal pull-up or pull-down resistors. When this feature is not used the SYNC pin should be grounded.

Shutdown

With V_{IN} applied and a logic LOW level on the $\overline{SD}$ pin, the converter is in shutdown mode. Shutdown mode is designed to reduce power consumption to a minimum level lowering supply current to less than 2 μA. This is accomplished by shutting off all of the circuits including the PMOS and NMOS switches. A logic HIGH enables the IC to start up as described in the start-up section.

Thermal Shutdown

The Si9174 includes thermal shutdown circuitry that turns off the regulator when the junction temperature exceeds 165°C. Once the junction temperature drops below 145°C, the regulator is re-enabled. If the overstress causing the temperature rise continues, the Si9174 begins thermal cycling, turning the regulator on and off in response to junction temperature. Restart from a thermal shutdown condition is the same as described in the start-up section.

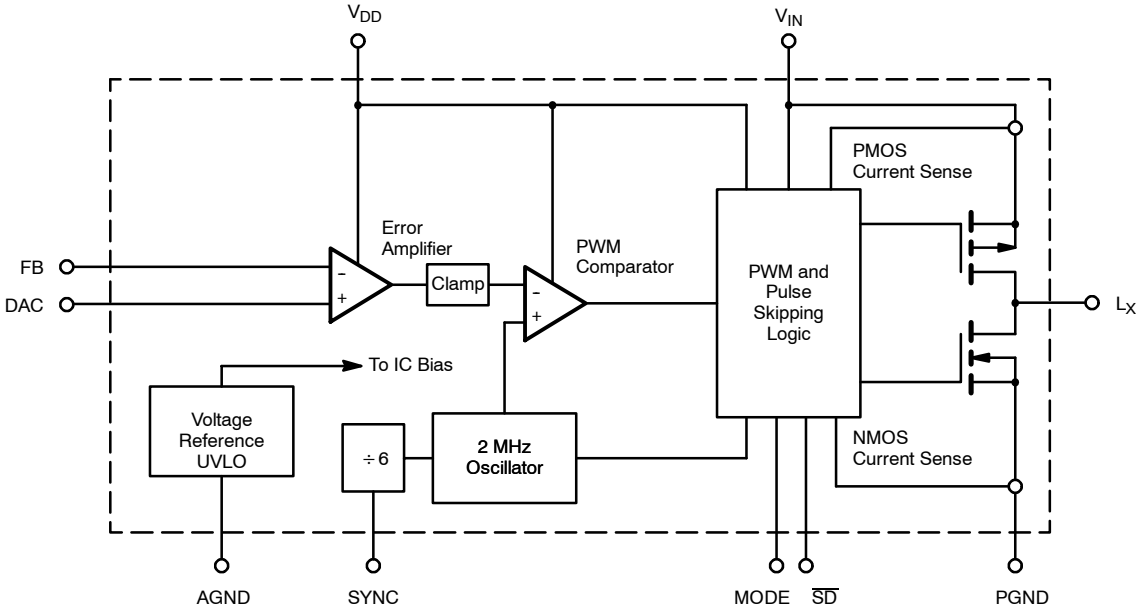


Figure 6. Si9174 Functional Block Diagram

DESIGNING WITH THE Si9174/75/76

The internal compensation of the Si9174/75/76 devices simplifies converter designs and reduces total component count to just six active and passive devices. Their 2-MHz switching frequency, moreover, gives the designer the ability to minimize inductor and capacitor sizes.

Setting the Output Voltage on Si9174

The DAC input on the Si9174 is used to dynamically adjust the output voltage. The Feedback (FB) pin voltage is regulated to the same voltage level as the DAC pin. Two resistors set the gain from the DAC pin to the V_{OUT} voltage. For V_{DAC} voltages within the specified voltage range of 0.28 to 2.45 V, V_{OUT} is proportional to V_{DAC} according to the following relationship:

$$V_{OUT} = V_{DAC} * \left(1 + \frac{R1}{R2}\right) \quad (1)$$

To minimize the current consumed by the voltage divider and isolate the FB pin from switching noise, the resistor values for R_1 and R_2 should be between 5 kΩ and 100 kΩ.

Setting the Output Voltage on Si9175 and Si9176

The output voltage of the Si9175 and Si9176 is set with a fixed resistor divider feedback network. The voltage output can be set between V_{REF} and ($V_{IN} - V_{DROP}$) where V_{DROP} is the voltage drop across the 0.3 Ω p-channel MOSFET in 100% duty cycle. V_{OUT} is defined by the following relationship:

$$V_{OUT} = V_{REF} * \left(1 + \frac{R1}{R2}\right) \quad (2)$$

The internal reference voltage, $V_{REF,}$ is 1.215 V. To minimize the current consumed by the voltage divider and to isolate the FB pin from switching noise, the resistor values for R_1 and R_2 should be between 5 kΩ and 100 kΩ. No connection should be made to the REF pin.

INDUCTOR AND OUTPUT CAPACITOR SELECTION

The Si9174/5/6 family uses internal Type III lead-lag compensation circuitry. While internal compensation simplifies the system level design and reduces the number of external components, it limits the range of values for the inductor and output capacitor.

The output inductor and capacitor must have a resonant frequency of 50 kHz to ensure loop stability. The LC resonant frequency is defined by the following equation:

$$f = \frac{1}{2\pi\sqrt{LC}} \quad (3)$$

INDUCTOR SELECTION

The internal compensation circuitry requires that the inductor values range from 1.5 μH to 4.7 μH. When selecting the inductor, the inductor value, dc resistance (DCR), and saturation current are the primary parameters to consider. Inductor values in the lower end of the specified range require larger capacitor values to keep the resonant frequency constant. Larger capacitor values minimize the voltage ripple.

Smaller inductor values typically have a lower value of DCR, which improves efficiency. It is desirable to minimize the dc resistance because it represents power loss and therefore reduced efficiency. The impact of DCR on efficiency is a function of output current. The DCR range can vary significantly, for example from 20 mΩ to 250 mΩ, which can result in as much as a 6% loss in efficiency in a 1-W application. As shown in Table 1, the lower the DCR, the larger the physical size of the inductor.

It is important to prevent the inductor core from saturating. Saturation will reduce the inductance and increase the dc resistance. Reduced inductance may cause instability and the increase in DCR will result in a loss of efficiency.

The saturation current rating of the inductor should be 1.6 times larger than the maximum output current.

If small physical size of an inductor is paramount but the dc resistance is too high and the saturation current is too low, it is possible to parallel two inductors to reduce the total DCR in half while doubling the total current capability. This allows designers to use the smaller form-factor chip inductors while still meeting the required load current and efficiency design objectives.

TABLE 1
Inductor Selection

Manufacturer	Part Number	Inductance (µH)	DCR (mΩ)	Max DC Current (A)	Dimensions (mm)
TOKO	A914BYW-2R2M	2.2	59	1.63	5X5X2
	A914BYW-4R7M	4.7	87	1.14	5X5X2
Taiyo Yuden	LB2518B 2R2M	2.2	130	0.340	2.5X1.8 (805)
	LB2518B 4R7M	4.7	250	0.240	2.5X1.8 (805)
Coilcraft	DO1608 222	2.2	80	1.8	6.6X4.45X2.9
	D01608 472	4.7	120	1.4	6.6X4.45X2.9
Vishay	IHLP-2525	1.5	2.5	60	6.8X6.5X3
	IHLP-2525	2.2	20	14	6.8X6.5X3
	IHLP-2525	4.7	40	10	6.8X6.5X3

Output Capacitor Selection

Once the inductor value is selected, the output capacitor value is selected by keeping the resonant frequency at 50 kHz.

$$C = \left(\frac{1}{2\pi f}\right)^2 * \frac{1}{L} \quad (4)$$

where f = 50 kHz

For the inductor ranges described above, corresponding capacitor values are shown below in Table 2. If the value listed is not available, select the closest possible value, allowing a small increase in the resonant frequency.

TABLE 2
Output Capacitor Selection

Inductor Value	Capacitor Value
1.5uH	6.8uF
2.2uH	4.7uF
3.3uH	3.0uF
4.7uH	2.2uF

Low-ESR ceramic capacitors are required on the output to keep the output voltage ripple small and to ensure that the regulation control loop is stable.

TABLE 3
Output Capacitor Selection

Value (µF)	Capacitor Type	ESR (mΩ)
2.2 – 6.8	16V MLCC	< 50

Input Capacitor Selection

To minimize current pulse induced ripple caused by the step-down converter and interference of large voltage spikes from other circuits, a low-ESR input capacitor is required to filter the input voltage.

The input capacitor should be rated for the maximum RMS input current:

$$I_{RMS} = I_{LOAD(MAX)} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

It is common practice to rate for the worst-case RMS ripple that occurs when the duty cycle is at 50%:

$$I_{RMS} = \frac{I_{LOAD(MAX)}}{2} \quad (6)$$

Ceramic capacitors are recommended for use as the input capacitor because of their low ESR and reduced sensitivity to voltage transients as compared to tantalum capacitors.

The minimum recommended value for the input capacitor is 4.7 µF. This value can be increased for better input voltage filtering. An additional 0.01 µF is also recommended in parallel with the bulk capacitor on V_{IN} for high-frequency decoupling. Depending on noise generated on the PC board, a 0.01-µF capacitor may be required between AGND (pin 2) and the V_{DD} pin (pin 4) to minimize noise that can impact the IC control circuit.

TABLE 4
Input Capacitor Selection

Value (µF)	Type	ESR (mΩ)
4.7 - 10	16V MLCC	< 150
0.01 – 0.1	16V MLCC	< 150

IMPLEMENTING DYNAMIC CONTROL OF V_{OUT} WHEN USING THE SI9175/76

The Si9175 and Si9176 do not have a DAC input to dynamically control the output voltage, yet the output can still be dynamically controlled by a V_{ADJ} signal as shown in Figure 7.

The FB node is now the summing node between the V_{OUT} and V_{ADJ}. Note that the output voltage decreases for increasing V_{ADJ}.

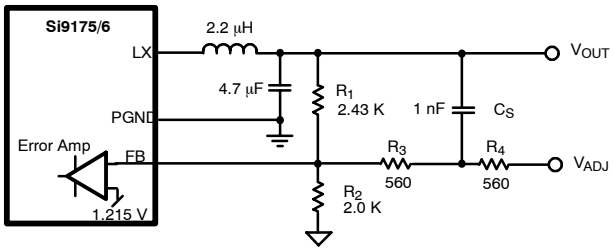


Figure 7. Dynamic Control of the Si9175/6

The general equation defining V_{OUT} is:

$$V_{OUT} = 1.215 * \left(1 + \frac{R1}{R2} + \frac{R1}{R_{ADJ}} - \frac{V_{ADJ} * R1}{R_{ADJ}}\right) \quad (7)$$

where $R_{ADJ} = R3 + R4$

This configuration allows output voltage to be lower than the reference voltage of the converter. The C_s capacitor is used to improve the transient response. Figure 8 shows the output waveform without capacitor. Figure 9 is the waveform with a 1-nF capacitor.

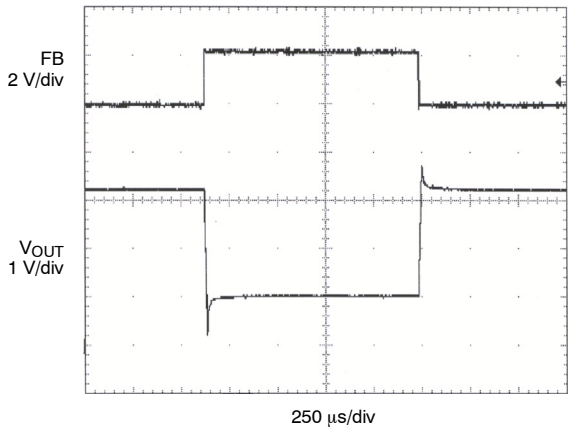


Figure 8. Transient response with no capacitor

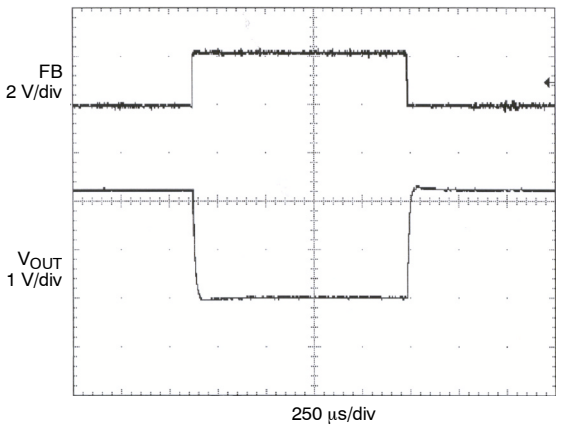


Figure 9. Transient Response with C_s capacitor = 1 nF

Implementing a TWO State Dynamic V_{out} when using the Si9175/6

When two precise V_{OUT} voltages are required (as in low-power DSP applications) the Si9175/6 can be configured with parallel load resistors on the feedback divider. One of the parallel resistors will be connected to the drain of a NMOS switch that can be switched by a control signal.The general equations for the two states are:

For Control = LOW

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) * 1.215V \quad (8)$$

For Control = HIGH

$$V_{OUT} = \left(1 + \frac{R1}{R2 \parallel R3}\right) * 1.215V \quad (9)$$

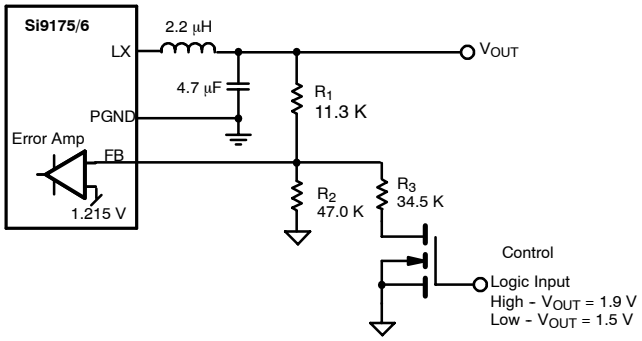


Figure 10. Two State Dynamic Control of V_{OUT}

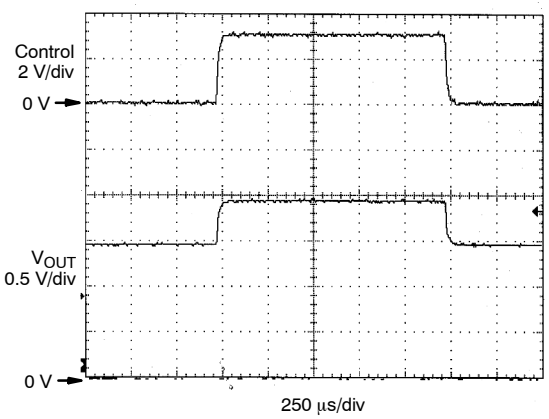


Figure 11. Two State Dynamic Control Waveforms

PCB LAYOUT CONSIDERATIONS

As in the design of any switching dc-to-dc converter, careful layout will ensure that there is a successful transition from design to production. One of the few drawbacks of switching dc-to-dc converters is the noise induced by their high-frequency switching. Parasitic inductance and capacitance may become significant when a converter is switching at megahertz frequencies. However, noise levels can be minimized by properly laying out the components. Here are some general guidelines for laying out a step-down converter with the Si9174/5/6 family.

Since most power traces in step down converters carry pulsating current, energy stored in trace inductance during the pulse can cause high-frequency ringing with input and output capacitors. Minimizing the length of the power traces will minimize the parasitic inductance in the trace. The same pulsating currents can cause voltage drops due to the trace resistance and cause effects such as ground bounce. Increasing the width of the power trace, which increases the cross sectional area, will minimize the trace resistance.

In all dc-to-dc converters the decoupling capacitors should be placed as close as possible to the pins being decoupled to reduce the noise. The connections to both terminals should be as short as possible with low-inductance (wide) traces. These traces are shown as heavy lines in Figure 12. In the Si9174/5/6 converters, the V_{IN} is decoupled to PGND. It may be necessary to decouple V_{DD} to AGND, with the decoupling capacitor being placed adjacent to the pin.

AGND and PGND traces should be isolated from each other and only connected at a single node such as a “star ground”. An example of this is shown in Figure 12.

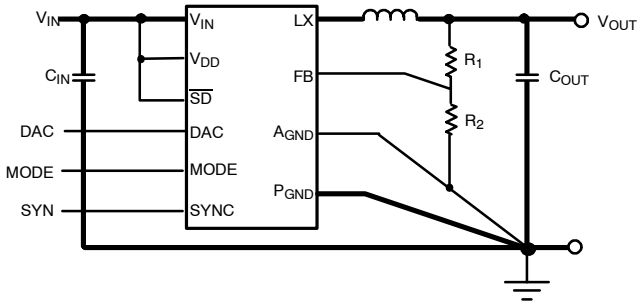


Figure 12. Si9174/5/6 Schematic

DEMO BOARDS

There are two demo boards available for the Si9174/5/6 family. The Si9174DB is the demo board part number for the Si9174 device and the Si9175/6DB is the demo board part number for both the Si9175 and Si9176 due to their similarities.

Si9174 Demo Board

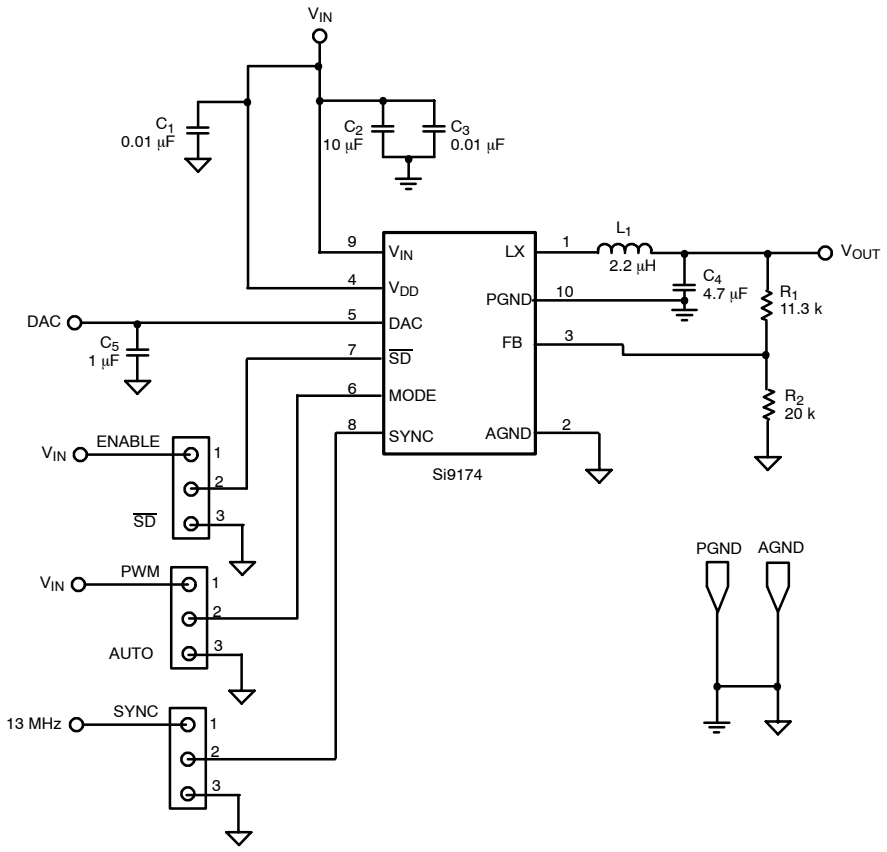


Figure 13. Si9174 Demo Board Schematic (Si9174DB)

TABLE 5
Si9174 Demo Board Schematic (Si9174DB)

Ref Des	QTY	Part Number	Description	Manufacturer
C1, C3	2	VJ0402Y103KXJAB	0.01uF, 16V	Vishay
C2	1	GRM42-2X5R106K10	10uF	Murata
C4	1	GRM42-6X5R47516	4.7uF	Murata
C5	1	VJ0603Y104KXXXAT	0.1uF, 25V	Vishay
L1	1	A914BYW-2R2M	2.2uH	Toko
R1	1	CRCW04021132F	11.3K 1%	Vishay
R2	1	CRCW04022202F	20K 1%	Vishay
	9		1mm pin	
J1, J2, J3	3		3-Pin Header	
U1	1	Si9174	2MHz Step-down converter	Vishay Siliconix

Si9175/6 Demo Board

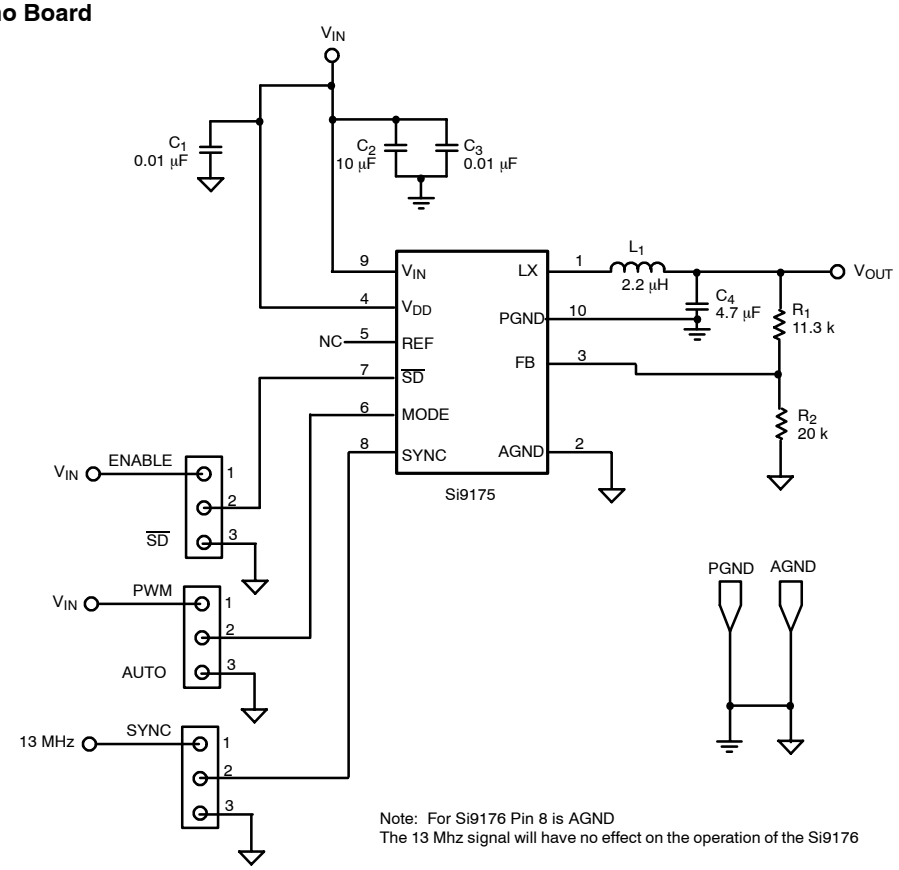


Figure 14. Si9175/6 Demo Board Schematic (Si9175/6DB)

TABLE 6
Si9175/6 Demo Board Schematic (Si9175/6DB)

Ref Des	QTY	Part Number	Description	Manufacturer
C1, C3	2	VJ0402Y103KXJAB	0.01uF, 16V	Vishay
C2	1	GRM42-2X5R106K10	10uF	Murata
C4	1	GRM42-6X5R47516	4.7uF	Murata
L1	1	A914BYW-2R2M	2.2uH	Toko
R1	1	CRCW04021132F	11.3K 1%	Vishay
R2	1	CRCW04022202F	20K 1%	Vishay
	9		1mm pin	
J1, J2, J3	3		3-Pin Header	
U1	1	Si9175	2MHz Step-down converter	Vishay Siliconix

Demo Board Set Up

The Si9174 and Si9175/6 demo boards come with the output voltage pre-set. The values of feedback resistors R_1 and R_2 have been selected for a gain of 1.565, which yields the following output voltages.

For the Si9174DB, V_{OUT} = DAC * 1.565
For the Si9175/6DB, V_{OUT} = 1.9 V

The Enable (EN) jumper is used to enable the device when the jumper connects pins 1 and 2. With the jumper across pins 2 and 3, the converter is shut down as covered in the Operational Description.

The PWM jumper is used to set the mode of operation. PWM mode of operation is set when the jumper is across pins 1 and 2. AUTO mode of operation is set when the jumper is across pins 2 and 3. PSM mode of operation is set when the jumper is removed and pin 2 is floating.

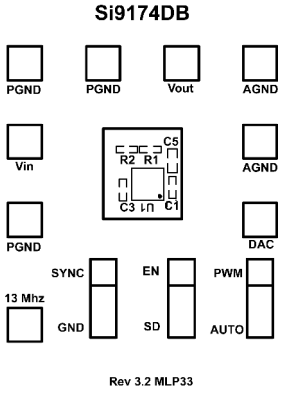
The SYNC jumper allows a 13-MHz sine wave signal to synchronize the internal oscillator when the jumper is across pins 1 and 2. If synchronization is not required, or if an Si9176 IC is used in the in the Si9175/6DB, the jumper should be set across pins 2 and 3, grounding the SYNC pin on the IC.

Demo Board Hook Up

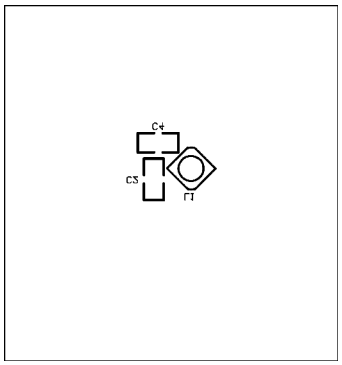
1. Connect power supply to the V_{IN} and PGND pins after presetting the supply's current limit.
2. Connect an electronic load or a resistive load across the V_{OUT} and PGND pins
3. Connect voltmeter or oscilloscope probe across the V_{OUT} and PGND pins
4. Connect a power supply or DAC signal to the DAC pin for the Si9174DB
5. Verify that enable jumper is in the EN position
6. Verify that the SYNC jumper is in the GND position unless synchronization with a 13-MHz signal is required.
7. The PWM jumper can be on the PWM position, the AUTO position, or removed for PSM mode.
8. Turn on power supply and verify that the current is not excessive.

PCB Layout

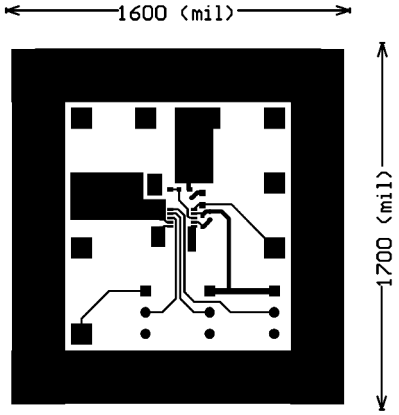
The demo boards were designed with two-sided component placement to minimize board area. Gerber files for the Si9174DB and the Si9175/6DB are available upon request.



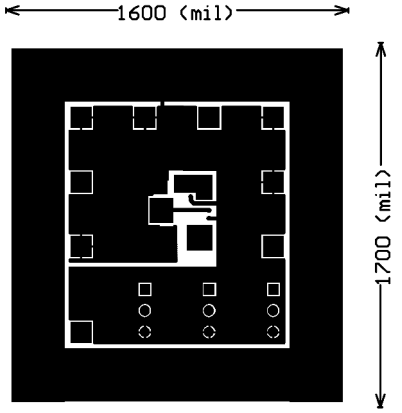
Top-Side Silkscreen



Bottom-Side Silkscreen

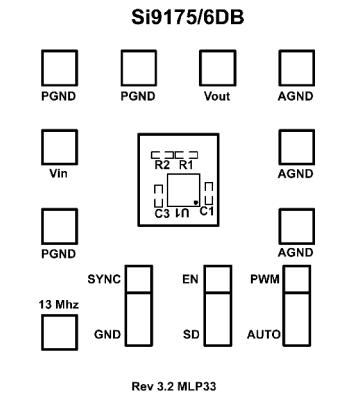


Top-Side Copper

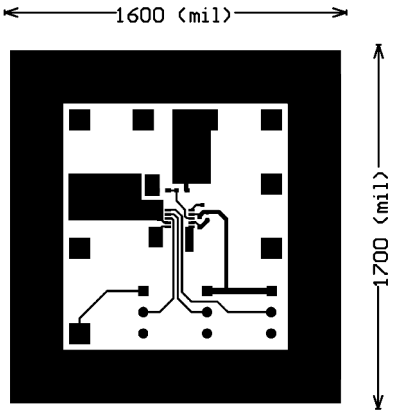


Bottom-Side Copper

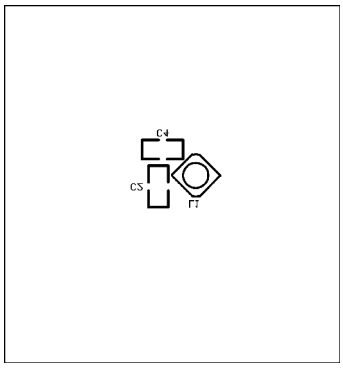
Figure 15. Si9174 Demo Board Artwork



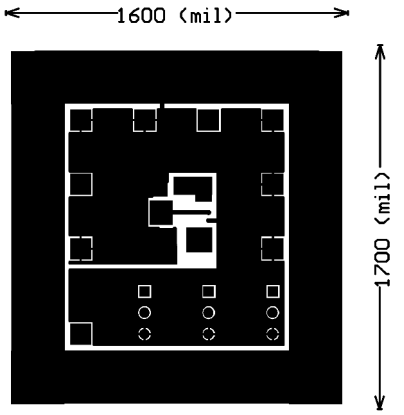
Top-Side Silkscreen



Top-Side Copper



Bottom-Side Silkscreen



Bottom-Side Copper

Figure 16. Si9175/6 Demo Board Artwork

MANUFACTURER'S WEB SITES

The following table contains the web addresses of the inductor manufacturers mentioned.

Manufacturer	Web Site
TOKO	www.tokoam.com
Taiyo Yuden	www.t-yuden.com
Coilcraft	www.coilcraft.com
Vishay	www.vishay.com